Fully Integrated Wide Input Voltage Range Capacitive DC-DC Converters: The Folding Dickson Converter

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***Abstract*—This paper presents a modified Dickson converter to achieve wide input range capacitive DC-DC converters. Several implementations are carefully studied and compared, which shows that the folding Dickson converter is the best choice, not only for its reduced dynamic losses, but also for its very regular structure and operation. Folding is achieved by merging the terminals of two or more flying capacitors, creating one equivalent flying capacitor. In this design, a four stage folding Dickson converter is implemented to achieve four different voltage conversion ratios. A Bootstrapped Gate Boost Converter (BGBC) is proposed which uses a bootstrapping technique to generate a floating rail for the flying switches, whose terminal voltages vary by large amounts depending on input voltage and VCR. The inherent operation of the Dickson topology is used by copying the voltage of the flying capacitors on a grounded capacitor in one phase, which can then be used to generate a floating 1.2V in the second phase. The converter has been implemented in a 90nm technology, achieving a maximum output power of 50mW, peak efficiency of 76.6% in the 2:1 conversion mode, and an average efficiency above 60% over the entire Vin and Pout range.**

***Index Terms*—monolithic, wide input-range, SC-DCDC, folding, Dickson, switched capacitor**

I. Introduction

FULLY integrated capacitive DC-DC converters have been on the rise for several years. Since capacitive converters have been brought under the attention of academia in [1] as a viable alternative for inductive converters, the number of publications on this topic has risen drastically (see Fig. 1). To this day, this research has given us high power density designs in bulk CMOS [2], [3], even higher power densities when using exotic capacitor types such as trench capacitors [4], [5] or ferroelectric capacitors [6], designs with very fast load transients [5], [7], extremely low ripple designs [8], highly integrated designs as in [9], [10], and even in the world of discrete SMP supplies, capacitive converters are under the spotlight [11]–[13], since in theory capacitive converters can outperform inductive converters [1], [9]. Some effort has also been done to fully integrate inductive converters [14], [15], but they either require extra process steps to have access to good quality inductors, or suffer from the parasitics of on-chip inductors which limit the achievable efficiency.

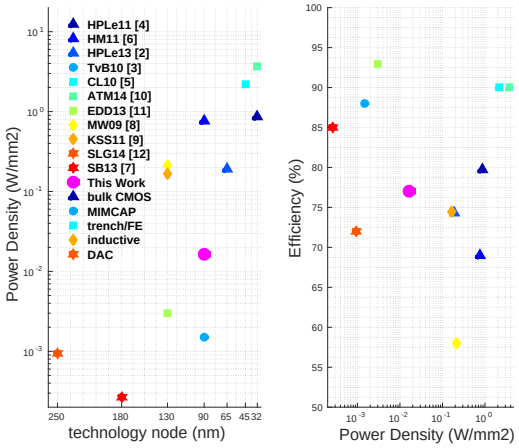


Fig. 1. Comparison of state-of-the-art fully integrated designs regarding power density, technology node and efficiency.

Most switched capacitor designs employ some kind of gearboxing or gain hopping, to overcome the theoretical upper limit on efficiency of these converters. Examples of this are found in [2], [5]–[8], [16], but are usually limited to 2-3 voltage conversion ratios (VCR), and do not stray far from the V_{dd} of the technology. The designs in [17], [18] take gearboxing one step further, and employ DAC-like techniques to deliver a very fine resolution switched capacitor converter, but are limited in output power, and input voltage is roughly limited to the V_{dd} of their technology. In [9], a highly integrated converter is proposed that also performs a gearboxing operation to achieve wide input voltage range operation, but changing the VCR comes at the cost of bypassing part of the converter, which can not be justified in a fully integrated design, where usually capacitors are a scarce resource, and bypassing would have a severe impact, especially so for low conversion ratios.

This paper proposes to use the Dickson converter as a wide input range capacitive converter: its very regular structure allows its stages to be folded into each other, creating from several flying capacitors, one lumped flying capacitor. This allows the converter to operate in several conversion ratios with full use of all of the flying capacitors.

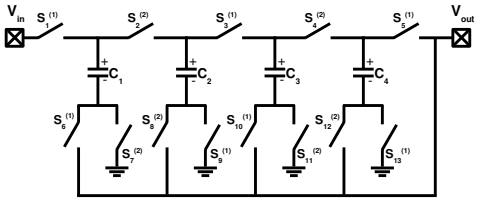


Fig. 2. Four stage Dickson converter, realising a 5:1 step-down conversion ratio.

The outline of this paper is as follows: in Section II the Dickson topology is introduced, and several gearboxing approaches are examined. A charge vector analysis is followed by an in-depth power loss analysis across all approaches. After justifying the choice for the folding Dickson converter, Section III goes into the details of the design and implementation of the proposed converter. Sizing of the switches, used transistor types, and multiphase interleaving are discussed. Next, the challenges for driving the floating switches of the folding Dickson converter are explained. The operation of the proposed bootstrapped gate boost converter is discussed. Section IV discusses the measurement results of the fabricated design, before drawing the conclusions in Section V.

II. Topological Analysis

The Dickson converter made its first appearance in 1976 [19], where it was proposed as an improvement over the Cockroft-Walton voltage multiplier, due to its relative insensitivity towards stray capacitance to achieve efficient voltage multiplication, together with its superior output current driving capability. Small changes were made to the topology, such as replacing the diodes by actively driven switches, overcoming the often limiting V_T drop of the diode-coupled MOSFETs. Nowadays, the topology still enjoys a lot of attention in literature and state-of-the-art designs [9], [11]–[13].

An example of a 4-stage step-down Dickson converter can be seen in Fig. 2. By correctly alternating the phases at which the top plate and bottom plate connecting switches are activated, a 5:1 step-down conversion is achieved. Already it is seen that due to its very regular structure, any number of N serially connected stages realize an (N+1):1 conversion ratio.

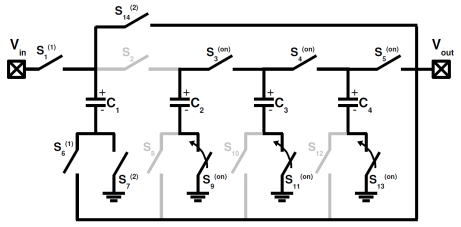
Using the same 4-stage 5:1 Dickson converter, there are several options to implement a 2:1 conversion ratio. These options are shown in Fig. 3(a), 3(b) and 3(c). Fig. 3(a) simply introduces an extra output tap via S_{14}, using C_1 and four switches to actively shuttle charge from the input to the output, while C_{2-4} are connected to the output in both phases, and act as extra decoupling capacitance. However, fully integrated designs are usually limited in the amount of flying capacitance available ($1 - 10's \frac{nF}{mm^2}$ for bulk CMOS [2], [3], [7], [16]), where discarding part of the flying capacitance would lead to a severe rise in switching frequency to maintain the same output impedance, especially for low conversion ratios.

The circuit in Fig. 3(b) overcomes this limitation by introducing additional switches S_{15-19}, hence using all the flying capacitance in the 2:1 mode. Another possibility is to use only the switches available in the standard 4-stage Dickson converter (Fig. 3(c)), and change the phase at which the switches are turned on. As such, switches S_{2-4} are kept on in both phases, and the bottom plate switches are driven in phase, resulting in the merging of C_{1-4} into one equivalent flying capacitor, which then performs a 2:1 conversion ratio. These three options will first be examined in a charge vector analysis, deriving topological constants K_c and K_s, after which a dynamic loss analysis will be performed to select the best of these three options.

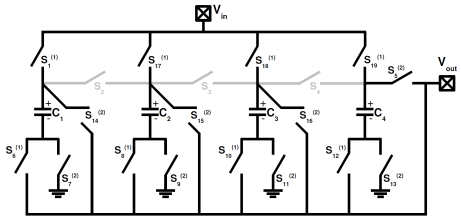
A. Charge Vector Analysis

A charge vector analysis is performed by inspecting both phases of the switched capacitor circuit, and determining the charges flowing in each of the branches of the circuit. These charges must respect Kirchhoff's current law, be equal but opposite in each phase for each capacitor, and be normalized so that $q_{out} = q_{out}^{\phi 1} + q_{out}^{\phi 2} = 1$. This method has been elaborately documented in [1].

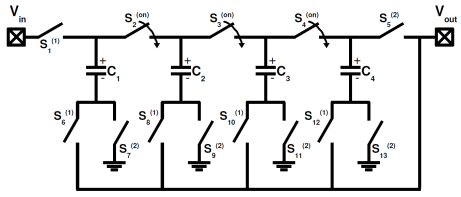
Taking a closer look at Fig. 3(a) and 3(b), it can be seen that these topologies have charge vector multipliers that are



(a) Four stage Dickson Converter using a variable output tap in 2:1-mode.



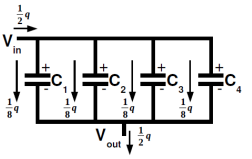
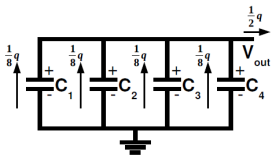
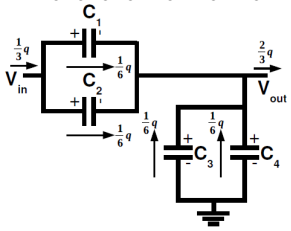
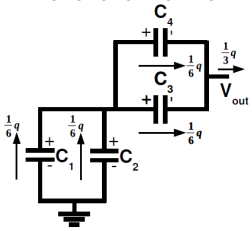
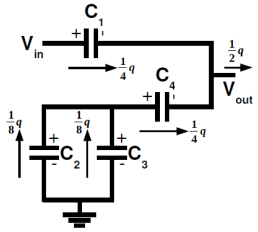
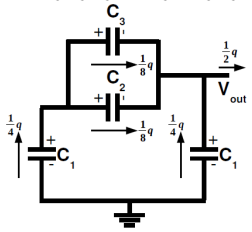
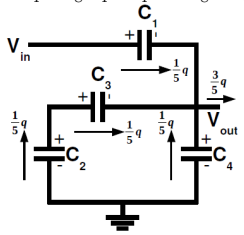
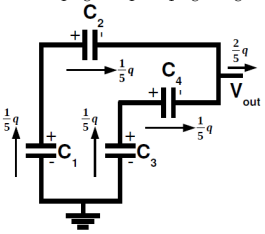
(b) Four Stage Dickson Converter using multiple input and output taps in 2:1-mode.



(c) Four stage Folding Dickson Converter in 2:1-mode.

Fig. 3. Three options to implement a multi-VCR Dickson Converter.

TABLE I
CHARGE FLOW ANALYSIS OF THE FOLDING DICKSON CONVERTER IN ITS FOUR VCRS.

VCR	ϕ_1	ϕ_2
$\frac{1}{2}$		
	$a_c(\phi_1) = [-\frac{1}{8}, -\frac{1}{8}, -\frac{1}{8}, -\frac{1}{8}]$	$a_c(\phi_2) = [\frac{1}{8}, \frac{1}{8}, \frac{1}{8}, \frac{1}{8}]$
	$a_r(\phi_1) = [\frac{4}{8}, \frac{3}{8}, \frac{2}{8}, \frac{1}{8}, 0 \mid \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0]$	$a_r(\phi_2) = [0, \frac{1}{8}, \frac{2}{8}, \frac{3}{8}, \frac{4}{8} \mid 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}, 0, \frac{1}{8}]$
$\frac{1}{3}$		
	$a_c(\phi_1) = [-\frac{1}{6}, -\frac{1}{6}, \frac{1}{6}, \frac{1}{6}]$	$a_c(\phi_2) = [\frac{1}{6}, \frac{1}{6}, -\frac{1}{6}, -\frac{1}{6}]$
	$a_r(\phi_1) = [\frac{2}{6}, \frac{1}{6}, 0, \frac{1}{6}, \frac{2}{6} \mid \frac{1}{6}, 0, \frac{1}{6}, 0, , 0\frac{1}{6}, 0, \frac{1}{6}]$	$a_r(\phi_2) = [0, \frac{1}{6}, \frac{2}{6}, \frac{1}{6}, 0 \mid 0, \frac{1}{6}, 0, \frac{1}{6}, \frac{1}{6}, 0, \frac{1}{6}, 0]$
$\frac{1}{4}$		
	$a_c(\phi_1) = [-\frac{1}{4}, \frac{1}{8}, \frac{1}{8}, -\frac{1}{4}]$	$a_c(\phi_2) = [\frac{1}{4}, -\frac{1}{8}, -\frac{1}{8}, \frac{1}{4}]$
	$a_r(\phi_1) = [\frac{1}{4}, 0, \frac{1}{8}, \frac{1}{4}, 0 \mid \frac{1}{4}, 0, 0, \frac{1}{8}, 0, \frac{1}{8}, \frac{1}{4}, 0]$	$a_r(\phi_2) = [0, \frac{1}{4}, \frac{1}{8}, 0, \frac{1}{4} \mid 0, \frac{1}{4}, \frac{1}{8}, 0, \frac{1}{8}, 0, 0, \frac{1}{4}]$
$\frac{1}{5}$		
	$a_c(\phi_1) = [-\frac{1}{5}, \frac{1}{5}, -\frac{1}{5}, \frac{1}{5}]$	$a_c(\phi_2) = [\frac{1}{5}, -\frac{1}{5}, \frac{1}{5}, -\frac{1}{5}]$
	$a_r(\phi_1) = [\frac{1}{5}, 0, \frac{1}{5}, 0, \frac{1}{5} \mid \frac{1}{5}, 0, 0, \frac{1}{5}, 0, \frac{1}{5}, 0, 0, \frac{1}{5}]$	$a_r(\phi_2) = [0, \frac{1}{5}, 0, \frac{1}{5}, 0 \mid 0, \frac{1}{5}, \frac{1}{5}, 0, 0, \frac{1}{5}, \frac{1}{5}, 0]$

essentialy those of a standard 2:1 VCR, with the major difference that the second option is actually four interleaved fragments in parallel of the same converter. Their charge multiplier vectors can be written as:

$$a_c = [\tfrac{1}{2}] \tag{1a}$$
$$a_r = [\tfrac{1}{2}, \tfrac{1}{2}, \tfrac{1}{2}, \tfrac{1}{2}] \tag{1b}$$

The other VCRs, such as the 3:1 and 4:1 conversion ratio, have indeed also the same charge vector multipliers as their standard implementations.

Fig. 3(c) however uses a different approach, which will be more closely examined using the figures of table I. In the case of the 2:1 VCR, each flying capacitor now only conducts $\frac{1}{8}$ of the total output charge. Switches S_{2-4} are connected in series during both phases, which causes them to conduct a total charge of $\frac{1}{2}$ summed over both phases. The resulting charge vector multipliers are as follows:

$$a_c = [\tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}] \tag{2a}$$
$$a_r(\phi_1) = [\tfrac{4}{8}, \tfrac{3}{8}, \tfrac{2}{8}, \tfrac{1}{8}, 0, \tfrac{1}{8}, 0, \tfrac{1}{8}, 0, \tfrac{1}{8}, 0, \tfrac{1}{8}, 0] \tag{2b}$$
$$a_r(\phi_2) = [0, \tfrac{1}{8}, \tfrac{2}{8}, \tfrac{3}{8}, \tfrac{4}{8}, 0, \tfrac{1}{8}, 0, \tfrac{1}{8}, 0, \tfrac{1}{8}, 0, \tfrac{1}{8}] \tag{2c}$$
$$a_r = [\tfrac{1}{2}, \tfrac{1}{2}, \tfrac{1}{2}, \tfrac{1}{2}, \tfrac{1}{2}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}, \tfrac{1}{8}] \tag{2d}$$

The same can be done for the Dickson converter in other 'folded' modes, which are shown in table I. Now that the charge multiplier vectors are available, their equivalent $K_c = (\sum_{i=1}^{n} a_c[i])^2$ and $K_s = (\sum_{i=1}^{n} a_r[i])^2$ factors can be calculated to perform a first order comparison. These factors are a measure of how efficiently a certain voltage conversion ratio

TABLE II
K_c AND K_s METRICS FOR THE STANDARD CONVERTER AND THE FOLDING DICKSON CONVERTER USING 4 FLYING CAPACITORS

Topology	$\mathbf{K_c}$	$\mathbf{K_s}$	$\mathbf{K_c}$ **F.D.**	$\mathbf{K_s}$ **F.D.**
$\mathbf{\frac{1}{2}}$	$\frac{1}{4}$	4	$\frac{1}{4}$	12.25
$\mathbf{\frac{1}{3}}$	$\frac{4}{9}$	5.44	$\frac{4}{9}$	9
$\mathbf{\frac{1}{4}}$	$\frac{9}{16}$	6.25	$\frac{9}{16}$	7.56
$\mathbf{\frac{1}{5}}$	$\frac{16}{25}$	6.76	$\frac{16}{25}$	6.76

TABLE III
APPROXIMATED TECHNOLOGY PARAMETERS USED FOR DYNAMIC LOSSES DEDUCTION, BASED ON ACTUAL MEASURED QUANTITIES.

parameter	$NMOS_{std}$	$NMOS_{I/O}$	$NMOS_{I/O@1.2V}$
μC_{ox}	K	$\frac{K}{2}$	K
gate length	L_{min}	$2L_{min}$	$2L_{min}$
V_{gs}	V_{dd}	$2V_{dd}$	V_{dd}
C_{gate}	C_{sq}	$\frac{C_{sq}}{2}$	$\frac{C_{sq}}{2}$

uses its capacitors (K_c) and its switches (K_s). Smaller values for these factors imply smaller capacitors and switches can be used to achieve a desired output impedance [1].

The results are shown in table II. It is clear that folding keeps the K_c metrics equal in both the standard case and the folded converter, whereas the K_s metric in the folding case suffers from an increase, which is due to the serialization of switches S_{2-4}, depending on the conversion ratio. These results will be used in the next paragraph, where we will continue the analysis by looking at the dynamic losses in the capacitive converters, before drawing our conclusions.

B. Loss Analysis and Comparison

Before going to the actual calculation of the dynamic losses, first the blocking voltages (the drain-source voltage the switches need to withstand in the phase that they are turned off) required for the switches must be investigated. Switches S_{6-13} are either connected to V_{out} or ground, allowing us to use standard V_{dd} devices. Switches S_{1-5} and S_{14-19} however, are connected to nodes other than the DC rails, and as such their required blocking voltage must be carefully investigated. In the 5:1 VCR, up to 8V is seen at the input for an output voltage of 1.2V. Fig. 4 shows the top plate voltages of the flying capacitors, along with the blocking voltage required for each switch. As can be seen, S_{1-5} can be implemented with a cascode of a standard device and an I/O-device, whereas the switches S_{14-19} introduced in Fig. 3(b) and 3(a) need up to 3 I/O-devices in cascode to enable safe operation in both the 2:1 as the 5:1 VCRs.

Next, the dynamic losses, namely $P_{C_{par}}$ (the parasitic bottom plate losses of the flying capacitors [20]) and P_{gate} (the losses associated with driving the switches [20]) will be calculated, which are given as:

$$P_{C_{par}} = f_{sw}(\sum_i \alpha C_i(\Delta V_{bp}^2)) \tag{3a}$$

$$P_{gate} = f_{sw}(\sum_j W_j L_j C_{sq}(V_{gs,j}^2)) \tag{3b}$$

Parameters R_{FSL} (Fast Switching Limit output impedance [1]) and R_{SSL} (Slow Switching Limit output impedance [1]) are assumed given, along with the technological constants given in table III. The flying capacitors are sized equally ($C_1 = C_2 = C_3 = C_4; \sum_{i=1}^{4} C_i = C_{tot}$), and all switches will be sized according to the charge multiplier vectors, as in [1].

1) Single output tap: In the first case, as seen in Fig. 3(a), only one flying capacitor is used to perform the power conversion. Hence:

$$f_{sw} = \frac{K_c}{R_{SSL}\frac{C_{tot}}{4}} = \frac{1}{R_{SSL}C_{tot}} \tag{4}$$

The conductance of each switch can be written down as follows, considering the cascoding of devices:

$$G_{tot} = \frac{2K_s}{R_{FSL}} = \frac{8}{R_{FSL}} \tag{5}$$

$$G_{6,7} = \frac{1}{4}G_{tot} \quad ; \quad G_{std,1} = G_{I/O,1} = \frac{2}{4}G_{tot} \tag{6}$$

$$G_{I/O,14} = \frac{3}{4}G_{tot} \tag{7}$$

The widths of the switches are then written down as such:

$$W_{6,7} = \frac{2}{R_{FSL}}\frac{L}{K(V_{GS}-V_T)} \tag{8}$$

$$W_{std,1} = 2\frac{2}{R_{FSL}}\frac{L}{K(V_{GS}-V_T)} \tag{9}$$

$$W_{I/O,1} = 2\frac{2}{R_{FSL}}\frac{2L}{K(V_{GS}-V_T)} \tag{10}$$

$$W_{I/O,14} = 3\frac{2}{R_{FSL}}\frac{2L}{K(V_{GS}-V_T)} \times 3 \tag{11}$$

Filling in these equations along with (4) into equation (3b) gives us the following expression:

$$P_{gate} = \frac{1}{R_{SSL}C_{tot}}\frac{160L^2}{R_{FSL}K(V_{GS}-V_T)}C_{sq}V_{dd}^2 \tag{12}$$

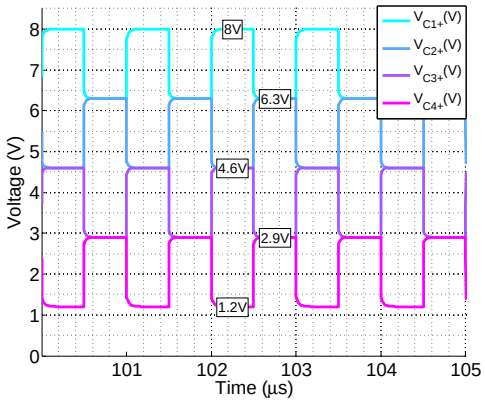
Similarly, the parasitic bottom plate losses can be found by combining equations (4) and (3a), realizing that $\Delta V_{bp} = V_{dd}$ for every flying capacitor in the Dickson converter:

$$P_{C_{par}} = \frac{1}{R_{SSL}C_{tot}}\alpha\frac{C_{tot}}{4}V_{dd}^2 = \frac{\alpha V_{dd}^2}{4R_{SSL}} \tag{13}$$

2) Multiple input and output taps: Next, consider the circuit in Fig. 3(b). The switching frequency is as follows:

$$f_{sw} = \frac{K_c}{R_{SSL}C_{tot}} = \frac{1}{4R_{SSL}C_{tot}} \tag{14}$$

Here, each flying capacitor can be seen as one of in total four interleaved fragments working in parallel. As such, the conductance of each individual switch can be four times



Switch	D	S	$V_{DS,\frac{1}{5}}$	impl.
M_1	V_{in}	V_{C_1+}	1.7V	std+I/O
M_2	V_{C_1+}	V_{C_2+}	3.4V	std+I/O
M_3	V_{C_2+}	V_{C_3+}	3.4V	std+I/O
M_4	V_{C_3+}	V_{C_4+}	3.4V	std+I/O
M_5	V_{C_4+}	V_{out}	1.7V	std+I/O
M_{14}	V_{C_1+}	V_{out}	6.8V	3*I/O
M_{15}	V_{C_2+}	V_{out}	5.1V	2*I/O
M_{16}	V_{C_3+}	V_{out}	3.4V	std+I/O
M_{17}	V_{in}	V_{C_2+}	3.4V	std+I/O
M_{18}	V_{in}	V_{C_3+}	5.1V	2*I/O
M_{19}	V_{in}	V_{C_4+}	6.8V	3*I/O

Fig. 4. Top plate voltages of the flying capacitors in 5:1-mode at an input voltage of 8V in the SSL-region, and the corresponding voltage rating requirements of the switches.

smaller to have the same total R_{FSL}.

$$G_{tot,frag} = \frac{1}{4}\frac{2K_s}{R_{FSL}} = \frac{2}{R_{FSL}} \tag{15}$$

$$G_{6-13} = \frac{1}{4}G_{tot,frag} \tag{16}$$

$$G_{std,1,5,16,17} = G_{I/O,1,5,16,17} = 2\frac{1}{4}G_{tot,frag} \tag{17}$$

$$G_{I/O,15,18} = 2\frac{1}{4}G_{tot,frag} \tag{18}$$

$$G_{I/O,14,19} = 3\frac{1}{4}G_{tot,frag} \tag{19}$$

The size of the switches can then be seen as follows:

$$W_{6-13} = \frac{1}{2R_{FSL}}\frac{L}{K(V_{GS}-V_T)} \tag{20}$$

$$W_{std,1,5,16,17} = \frac{1}{R_{FSL}}\frac{L}{K(V_{GS}-V_T)} \tag{21}$$

$$W_{I/O,1,5,16,17} = \frac{1}{R_{FSL}}\frac{2L}{K(V_{GS}-V_T)} \tag{22}$$

$$W_{I/O,15,18} = \frac{1}{R_{FSL}}\frac{2L}{\frac{K}{2}(2V_{GS}-V_T)} \times 2 \tag{23}$$

$$W_{I/O,14,19} = \frac{3}{2R_{FSL}}\frac{2L}{\frac{K}{2}(2V_{GS}-V_T)} \times 3 \tag{24}$$

Again, filling in these equations along with (14) into equation (3b) yields the following result:

$$P_{gate} = \frac{1}{R_{SSL}C_{tot}}\frac{30L^2}{R_{FSL}K(V_{GS}-V_T)}C_{sq}V_{dd}^2 \tag{25}$$

The parasitic bottom plate losses are now:

$$P_{C_{par}} = \frac{1}{4R_{SSL}C_{tot}}\alpha C_{tot}V_{dd}^2 = \frac{\alpha V_{dd}^2}{4R_{SSL}} \tag{26}$$

3) Folding Dickson Converter: The circuit in Fig. 3(c) differs from the previous circuits, namely due to folding operation explained in II, leading to an increase in K_s. Starting with defining the switching frequency, the following is found:

$$f_{sw} = \frac{K_c}{R_{SSL}C_{tot}} = \frac{1}{4R_{SSL}C_{tot}} \tag{27}$$

The required conductance of each switch can then be written as:

$$G_{tot} = \frac{2K_s}{R_{FSL}} = \frac{24.5}{R_{FSL}} \tag{28}$$

$$G_{std,1-5} = G_{I/O,1-5} = \frac{4}{28}G_{tot}; G_{6-13} = \frac{G_{tot}}{28} \tag{29}$$

With the switch sizes:

$$W_{std,1-5} = 2\frac{4}{28}\frac{24.5}{R_{FSL}}\frac{L}{K(V_{GS}-V_T)} \tag{30}$$

$$W_{I/O,1-5} = 2\frac{4}{28}\frac{24.5}{R_{FSL}}\frac{2L}{K(V_{GS}-V_T)} \tag{31}$$

$$W_{6,13} = \frac{1}{28}\frac{24.5}{R_{FSL}}\frac{L}{K(V_{GS}-V_T)} \tag{32}$$

These results can then be filled in to equation (3b) along with equation (27) to find the following expression for the gate losses:

$$P_{gate} = \frac{1}{R_{SSL}C_{tot}}\frac{12.25L^2}{R_{FSL}K(V_{GS}-V_T)}C_{sq}V_{dd}^2 \tag{33}$$

The parasitic bottom plate losses are now:

$$P_{C_{par}} = \frac{1}{4R_{SSL}C_{tot}}\alpha C_{tot}V_{dd}^2 = \frac{\alpha V_{dd}^2}{4R_{SSL}} \tag{34}$$

The first conclusion can be drawn by comparing the results of equations (13), (26) and (34), revealing that the parasitic bottom plate losses remain the same in all three circuits given a desired R_{SSL}.

Comparing the results of equations (12), (25) and (33) leads us to a much more interesting result. Here, it is seen that using the circuit of Fig. 3(a) is out of the question: the combination of a quadrupled switching frequency, along with the cascode of 3 I/O-devices to ensure valid operation, leads to very high dynamic losses to drive all of the switches. Interestingly, when comparing the other two circuits, we see that for a given R_{FSL} the folding Dickson converter achieves the lowest dynamic losses. It achieves this by being able to keep switches S_{2-4} on in both phases, meaning that these devices do not add to the dynamic losses. Another

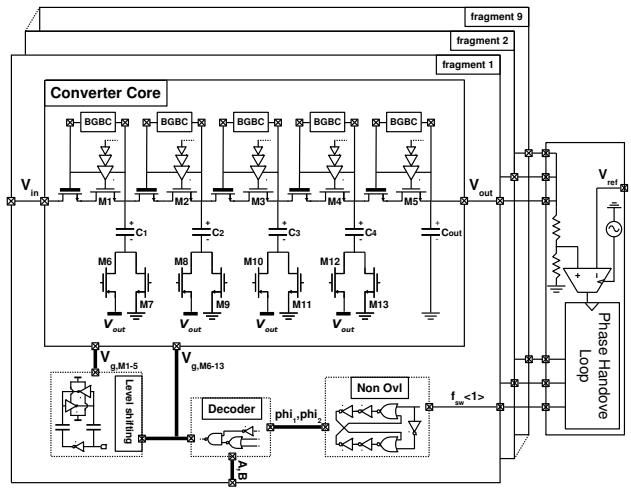


Fig. 5. System overview of the implemented design

key difference is that the folding Dickson converter only needs standard V_{dd} devices, or a cascode of a standard and an I/O-device, whereas the other circuit requires several switches implemented by a cascode of 2 or 3 I/O-devices. Note that in practice, the minimal gate length of an I/O-device can be up to 3-4 times the gate length of a standard device (whereas in the above calculation, a factor 2 has been conservatively assumed). Since the gate losses show a dependence $P_{gate} \sim L^2$, this can have a substantial influence on the absolute values of the gate losses. However, when comparing the gate losses of each circuit, the relative difference remains roughly the same.

Beside the obvious benefit in dynamic losses, other factors of a more practical nature lead us to the choice of the folding Dickson converter. Needing a cascode of 3 I/O-devices requires a complex biasing scheme to drive all devices with the correct voltages, requiring large passives, as in [21], or two supplies, $2V_{dd}$ and $4V_{dd}$ referenced to the source of the switch. On the other hand, in the case of the folding Dickson converter, the cascode devices simply need to be biased with a DC voltage equal to V_{dd}. The generation of this DC voltage will be explained in section III-C1.

III. Design and Implementation

An overview of the complete design can be seen in Fig. 5. In what follows, each part of the design of the converter will be discussed, starting with the requirements of each converter core, followed by the design of the control loop and required multiphase interleaving. In the last section, driving of the switches will be discussed, with extra attention for the Bootstrapped Gate Boost Converter (BGBC).

A. Converter Core

Some attention has already been given to the implementation choice of the switches in the converter. As said, switches S_{6-13} need to block only $V_{out} = V_{dd}$, allowing them to be implemented by standard NMOS and PMOS devices.

TABLE IV
Output impedance of each VCR as designed.

VCR	$R_{SSL,min}$	R_{FSL}	R_{out}	$\gamma_{P=50mw}$
$\frac{1}{2}$	1.25Ω	4.28Ω	4.46Ω	0.866
$\frac{1}{3}$	2.22Ω	2.77Ω	3.54Ω	0.89
$\frac{1}{4}$	2.81Ω	2.53Ω	3.78Ω	0.884
$\frac{1}{5}$	3.2Ω	2.24Ω	3.9Ω	0.88

However, switches S_{1-5} need to block up to 3.4V, which is shown in Fig. 4. In this design, a combination of a standard NMOS cascoded by a NMOS I/O-device allows us to block a total of 3.7V. Two reasons make this a better choice then simply cascoding 2 I/O-devices:
1) The dynamic losses for a given R_{on} are better in the case of cascoding a standard and an I/O-device. Furthermore, it is not required to give each device an equal R_{on}, so that the standard device can be given a smaller R_{on} than the I/O-device, to additionally reduce the total $\frac{P_{dyn}}{R_{on}}$. The difference in energy consumption per cycle can be as much as an order of magnitude.
2) The propagation delay of a standard device tapered buffer is shorter than that of an I/O-device tapered buffer. Together with the smaller capacitive load that the buffer needs to drive, a speedup of around 180% can be achieved, as has been suggested by simulations, for a given R_{on}.

Switches and capacitors have been sized for a maximum output power of 50mW. Since all switches are shared between the four different VCRs, four different sizing strategies for the switches have been experimented with, i.e. the sizing according to the charge multiplier vector of each VCR, which can be found in table I. It was found that sizing according to $VCR = \frac{1}{3}$ led to the highest overall efficiency seen over the entire input voltage range, while still providing adequate R_{FSL} in $VCR = \frac{1}{2}$. Flying capacitors are sized equally. The resulting output impedances of each VCR can be seen in table IV, which are calculated for a maximum switching frequency of 100MHz.

Switching frequency per fragment of the multiphase interleaved converter is generated by an on-chip hysteretic controller. This switching frequency is then fed into a standard non-overlapping clock generator. The resulting non-overlapping clocks phi_1 and phi_2 are then used alongside VCR bits A and B to generate the driving signals for each switch seperately. These driving signals are decoded using static CMOS logic. The propagation delay from non-overlapping clock signals to the actual driving signals is kept as low as possible, by keeping the number of stages down to two. The delay for decoding is around 50ps.
Since switches $S6-13$ reside in the voltage domain between ground and $V_{out} = V_{dd}$, no level shifting is required, and their driving signals can be fed into the tapered buffer driving the switch. The switching signals for switches S_{1-5} however need to be level shifted into their respective floating voltage domain, which is done by capacitive level shifters. These floating voltage domains are generated using the

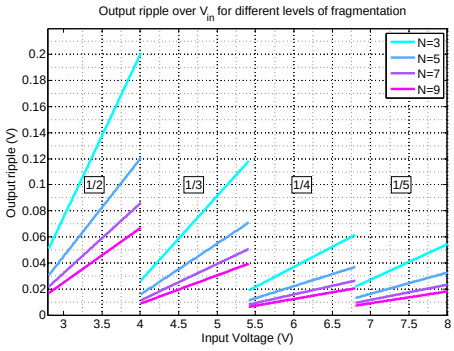


Fig. 6. Output ripple for different levels of multiphase interleaving and output capacitor of $C_{out} = 3nF$

Boostrapped Gate Boost Converter (BGBC), whose operation will be explained in section III-C.

On-chip input and output decoupling is added to the design. Input decoupling has been implemented by MOM capacitors, which have a higher breakdown voltage, while the output decoupling is done using MOSCAPs. Values for decoupling are $C_{in} = 670$pF and $C_{out} = 3$nF.

B. Fragmentation and control loop

To define the number of interleaved fragments that need to operate in parallel, the main criterion is the ripple on the output voltage. Pulse Frequency Modulation (PFM) is in many cases a good control strategy for capacitive DC-DC converters, due to the decrease in dynamic losses with decreasing switching frequency and ease of control. Controlling the converter with PFM does mean however that the ripple will increase for a given output power when decreasing the switching frequency, which can be approximated in the SSL-region by:

$$\Delta V_{out} = \frac{I_{load}}{f_{sw}\zeta N(C_{out} + k_\tau C_{fly})} \tag{35}$$

with I_{load} the output current, $\zeta = 1$ when the converter connects to the output in one phase, and $\zeta = 2$ when it connects to the output in both phases, N the number of interleaved fragments and k_τ a VCR defined constant, defining the minimal fraction of flying capacitance seen as decoupling capacitance. I_{load}, ζ, $k_\tau C_{fly}$ and f_{sw} have all been determined through the design of the converter for a specific maximum output power, leaving the freedom of two parameters, namely the number of interleaved fragments and the amount of output decoupling. Since each of the fragments is used in a fairly large range of input voltage ($1 \times V_{dd}$), care needs to be taken so that the ripple does not become exceedingly large. Fig. 6 shows an exploration of the ripple for this design for a fixed output capacitor of 3nF and several levels of multiphase interleaving. In the end, an output capacitor of 3nF along with a 9-level multiphase interleaving is chosen for this design, as this limits the ripple of the converter to roughly 5% of the output voltage.

The 9 interleaved fragments of the converter are controlled by a hysteretic loop, consisting of a resistive divider, and a dynamic comparator, generating the clock for a nine phase handover loop, similar to the control loop in [20]. Since a maximum switching frequency of 100MHz is chosen, the dynamic comparator must operate at 1.8GHz. The total delay of the control loop must as such be smaller than the period of the comparator clock, i.e. 556ps, so that the output voltage reacts before a next comparison is made.

C. Gate Drive Circuits

As said in the previous subsection, there is a stringent constraint on the total delay of the control loop. Since the propagation delay of the tapered buffer driving the switches is one of the largest contributors, the tapered buffers have been designed to have an equal driving strength per stage, to keep the total delay minimal. In our case, for the cascoded switch, the total propagation delay is 140ps or less, while in the case of a cascode of 2 I/O-devices, the delay would amount to 250ps. The other buffers are slightly faster since their capacitive load is smaller.

One main component of the converter design remains, and that is the bootstrapped gate boost circuit. It is roughly based on a circuit found in [22]. In what follows, the operation of this circuit will be discussed.

1) Bootstrapped Gate Boost Circuit: The BGBC can be seen in Fig. 7, where its two phase operation is shown, along with the voltages seen in the three stages of the converter, namely the input voltage $V_{Ch,x}-$, which is connected to the main converter's $C_{fly,x}$, the intermediate voltage V_{Ccp}, and the output voltage, $V_{Ch,x}+$. The BGBC consists of capacitor C_{cp}, which copies and stores the voltage on $C_{fly,x}+$, capacitor $C_{h,x}$, across which the charge for driving the flying switches is stored, and two pass devices, M_1 and M_2, which are are activated through bootstrapping capacitors $C_{bs,1-2}$. Each pass device consists of 3 transistors, 1 transistors which performs the conversion, and 2 helper transistor to bias the bulk of $M_{1,2}$ correctly.

$\mathbf{Phi_1}$: Assuming the voltage across $C_{bs,1}$ has been precharged to V_{Cfly} in the previous phase, this capacitor is boosted by $2 \times V_{out}$ to turn on pass device M_2, and C_{cp} is charged to $V_{Cfly} + V_{out}$. Note that in this phase, the bulks of M_1 and M_2 are connected to C_{cp}, both being lower than $V_{Ch,x}+$ and $V_{Ch,x}-$. In the meanwhile, $C_{bs,2}$ is being charged to the voltage over C_{cp}.

$\mathbf{Phi_2}$: Phase Phi_2 starts with the voltage at terminal $V_{Ch,x}-$ dropping by V_{out}, leaving an absolute voltage of V_{Cfly}. At this point, the voltage V_{Ccp} is approximately V_{out} higher than $V_{Ch,x}-$. When M_2 is now turned on via bootstrapping capacitor $C_{bs,2}$, C_{cp} discharges into $C_{h,x}$ untill an equilibrium is met, and the voltage across $C_{h,x}$ becomes:

$$\begin{aligned} V_{Ch,x} &= V_{Ch,x+} - V_{Ch,x-} \\ &= (V_{Cfly} + V_{out}) - (V_{Cfly}) - \Delta V \\ &= V_{out} - \Delta V \end{aligned} \tag{36}$$

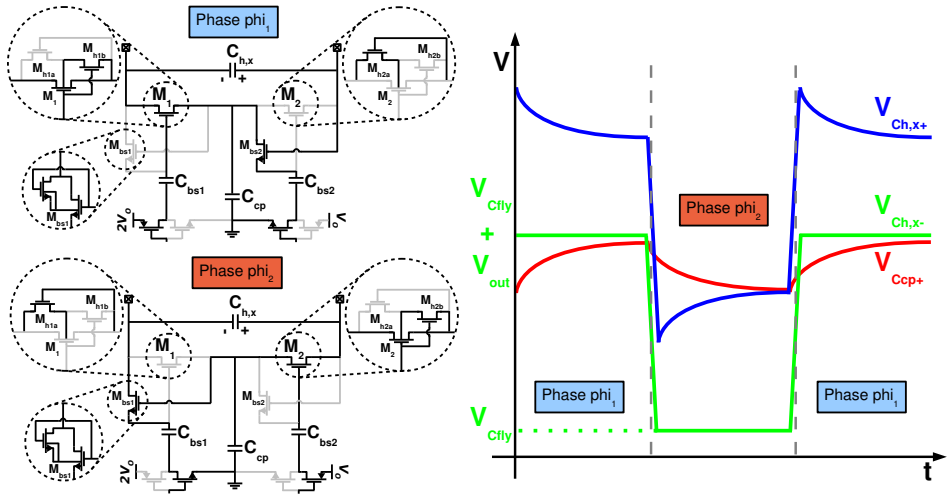


Fig. 7. Two phase operation of the Bootstrapped Gate Boost Circuit. The 2Vo is supplied externally.

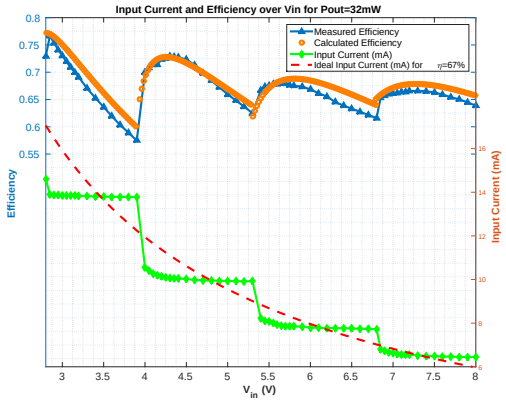


Fig. 8. Measured versus Calculated Efficiency, along with ideal and actual input current over the input voltage range, for $P_{out} = 32mW$

Which leaves us, depending on the sizing of $C_{h,x}$ and C_{cp}, with a voltage of roughly $V_{out} = 1.2V$ to drive the switches, since this voltage is referenced to the source of the switch (see Fig. 5). Note that in phase phi_2, the bulk of M_1 is connected to $C_{h,x}-$, and the bulk of M_2 to $C_{h,x}+$, which in both cases is the lowest voltage seen at source or drain of both devices. In this phase, $C_{bs,1}$ is also charged to the voltage V_{Cfly}, preparing for the operation of the next phase, which is again phi_1.

Since each of the stages of the Dickson converter works exactly the same, i.e. bottom plate connected to V_{out} in one phase, and to ground in the next, this building block can be used at every stage to generate this floating rail, making the operation of the converter very regular. This approach can be extended to any number of stages.

IV. Measurement Results

To validate the designed folding Dickson converter and confirm its operation, the four stage converter has been fabricated in a 90nm technology. The overview of the design can be seen in Fig. 5, and contains the 9 interleaved fragments controlled by an on-chip hysteretic controller, input and output decoupling. The input voltage range has been swept from 2.8V to 8V, having each VCR operate over a range of roughly 1.2V. This measurement is repeated across a power output range from 5mW to 50mW, being the designed maximum output power. The voltage at which VCRs are crossed over are kept constant.

As a first result, the upper part of Fig. 8 shows the comparison between the calculated efficiency and the actual efficiency, measured for an output power of 32mW. As can be seen, the measurements match closely to the calculated efficiency, which included bottom plate losses, gate losses and losses due to voltage swings on parasitic well capacitances. The lower part of the converter shows the measured input current of the converter, which for each VCR remains fairly constant after the initial switching frequency backoff. As an interesting comparison, the ideal input current of a generic power converter with an average efficiency of 67% is shown, which is also the average efficiency achieved by the Dickson converter at this output power. We can conclude that the folding Dickson converter, or in general wide input range capacitive DC-DC converters, are in fact a staircase approximation of this generic converter with idealized input current. The deviations from this line are the reason for the efficiency not being constant over the entire input range.

Fig. 9 shows the contour plot of the measured efficiency over the entire input voltage and output power range. It can be seen that the converter achieves its highest efficiency in the 2:1 converter mode of $> 74\%$ over a large part of the output power range, while still an acceptable efficiency can be seen for the other VCRs operating at higher input voltages. At $V_{in} = 4V$, the converter efficiency drops slightly below 60%, since at this point, the maximum efficiency is limited by $\gamma = \frac{V_o}{V_{in} VCR}$ (the theoretical efficiency [20]),

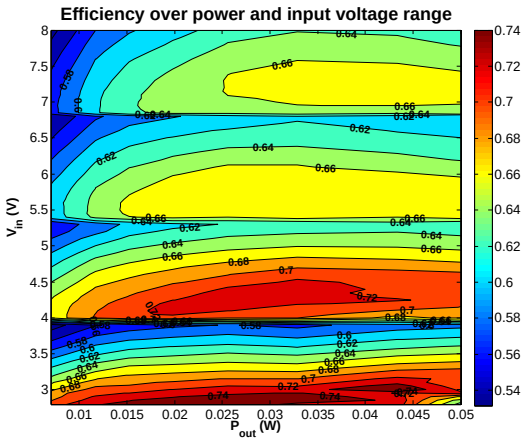


Fig. 9. Measured efficiency contour plot over V_{in} and P_{out}.

TABLE V
MAXIMUM EFFICIENCY OBSERVED, AT GIVEN INPUT VOLTAGE AND SWITCHING FREQUENCY.

VCR	η_{max}	$P_{out@\eta_{max}}$	V_{in}	f_{sw}
$\frac{1}{2}$	76.6%	32mW	2.85V	60MHz
$\frac{1}{3}$	73.1%	25mW	4.25V	30MHz
$\frac{1}{4}$	67.9%	32mW	5.4V	32MHz
$\frac{1}{5}$	66.6%	32mW	7.3V	64MHz

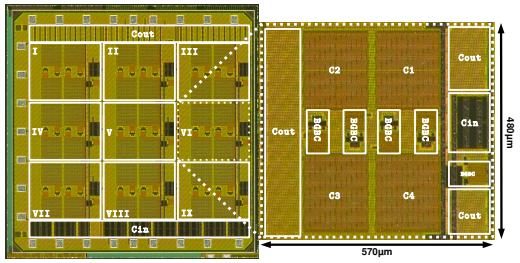


Fig. 10. Die photo of the fabricated design.

which is 0.6 at this input voltage.

Fig. 11 shows the Efficiency Enhancement Factor (EEF) over the same ranges, which is a measure for the improvement in efficiency compared to a linear regulator working at the same input and output voltage. A positive EEF would result in e.g. increased autonomy for battery powered applications [23]. Although efficiency is lowest in the 5:1 converter mode, it is in this range that the highest improvement is seen over a linear regulator, which would barely achieve 15-18% power efficiency in this input voltage range. An EEF of up to 50% has been achieved, with a minimum of 22%.

To conclude, the maximum efficiency for each converter mode is shown in table V, together with the switching frequency and input voltage at which this maximum efficiency occurs. The die photo of the fabricated design can be seen in Fig. 10. A comparison with the state-of-the-art is made in table VI, as well as in figure 1.

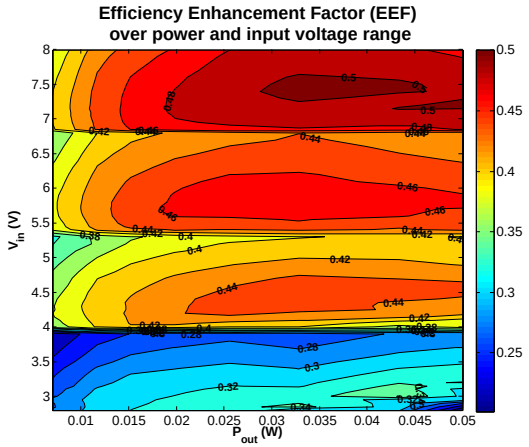


Fig. 11. Measured Efficiency Enhancement Factor (EEF) contour plot over V_{in} and P_{out}.

V. CONCLUSION

This paper discussed the design, implementation and measurement of the folding Dickson converter, fabricated in a 90nm technology. By exploiting the inherent operation of the Dickson converter and its very regular structure, four different Voltage Conversion Ratios (VCRs) can be implemented over an input voltage range of more than $4 \times V_{dd}$, achieving a peak efficiency of 76.6% in the 2:1 converter mode, and an acceptable efficiency over a wide input voltage range. Especially at the higher input voltage range, there is a clear benefit over standard linear regulator designs. Having each VCR operate over $1 \times V_{dd}$ requires extra attention to be given regarding ripple, which can be coped with by providing adequate multiphase interleaving and decoupling. The principle of folding can be extended to any number of stages, thanks to the aforementioned regularity of the folding Dickson topology.

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TABLE VI
COMPARISON WITH STATE-OF-THE-ART

Work	**[7]**	**[16]**	**[18]**	**[8]**	**[24]**	**This work**
technology	65nm LP CMOS	90nm CMOS	0.25μm CMOS	90nm CMOS	28nm FD-SOI	90nm CMOS
$VCRs$	$\frac{2}{5},\frac{1}{3}$	$\frac{4}{5},\frac{2}{3}$	4-bit recursive	$\frac{2}{3},\frac{1}{2}$	$\frac{5}{2},\frac{2}{1},\frac{3}{2}$	$\mathbf{\frac{1}{2},\frac{1}{3},\frac{1}{4},\frac{1}{5}}$
C_{fly}	3.88nF MOS	MIM	3nF MIM	1.15nF MO(M/S)	MO(M/S)	2nF MIM
ρ (mW/mm2)	190	1.51	0.94	38.6	4.9	16.3
η_{peak}	74.3%	88%	85%	81%	88%	76.6%
V_{out}	1V	0.5-0.85V	0.1-2.18V	0.7V	1.2-2.4V	1.2V
V_{in}	3-4V	0.7-1.2V	2.5	1.2-2V	1V	**2.8-8V**

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